Mohamed Matar

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Graduate research assistant focusing on **machine learning** and **5G networks** hardware accelerators in the university of British Columbia, experienced digital design and verification with ***five*** years of experience in academia and industry, and teaching experience of relevant courses.

Previous Employment

- **Research Assistant** **Vancouver**

  University of British Columbia, Canada *Jan 2018 – Now*

  ***Thesis*: Design exploration of Faster than Nyquist Equalizer. (Co-supervised by Mieszko Lis/Lutz Lampe)**

  In this work, we explored the design space of the next-generation Faster-than-Nyquist communications hardware accelerator composed of a MAP equalizer and an LDPC decoder. We proposed a highly configurable architecture to study the various trade-offs. We developed a MATLAB based bit-accurate system model, and a high level synthesis FPGA design that is evaluated on an Ultrascale+ FPGA.

  Part of this work was published in **FCCM 2020** conference (*check publication section*).

  Analysis of DNN Accelerator in SoC simulator.

  In this work, we integrated a DNN simulator with gem5 system simulator to measure the system performance with DNN workloads. DNN engine is connected on the system bus through memory mapped interface. We integrated NN APIs to run C++ based DNN workloads along with host code. In this *report*, we analyzed DNN workloads performance by running different CNN networks and measure kernel launch latency as well as DNN latency.

  DropBack: Continous Pruning During Training GPU implementation.

  Dropback pruning *paper* introduces an algorithm to regenerate weights during training instead of loading them from DRAM as a way to save energy. In this work, we implemented this algorithm on cutlass (Nvidia's open kernels for MatMul) and compare it with CuDNN (Cuda DNN engine using MAtMul).

- **Design Verification Engineer** **Penang**

  Intel Corporation, Malaysia *Feb 2016 – Jan 2018*

  Verification of MIPI-Audiolink IP

  As a part of mixed signal group, I was responsible for ownership of validation MIPI-audiolink IP. This IP was part of different Intel processor chips such as Cannon-lake, Ice-lake and Tiger-lake architectures. This required developing OVM based test cases, running RTL regressions, GLS simulations and measuring functional and code coverage.

Design Verification Engineer **Selangor**

Symmid Corporation, Malaysia *Feb 2016 – Jan 2017*

Non Volatile Flash Memory with AHB-APB Interface Verification

In this project, I was working with another colleague to develop a UVM based enviroment to test an ECC flash memory interface. This memory uses AHB-ABP interfaces to be integrated with ARM based SoC. This included contributing to the test plan, developing UVM components and test-cases, running RTL regressions, GLS debugging, and measuring functional and code coverage.

Research Assistant **Cairo**

American University in Cairo, Egypt *Jan 2015 – Feb 2016*

Modifying Virtual Memory Architecture to Enhance STT-RAM Performance STT-RAM is a magnetic based RAM that's considered as a potential replacement for DRAM. Due to its high write power, we introduce an operating system solution to reduce the writing energy. Our method introduces a page replacement policy that can reduce the number of bit write operations and consequently reduce the overall power consumption. This is done by using a simple hashing algorithm to select the target page with the nearest distance. We reflected this method on linux kernel, Gem5 full system simulator and a modified NVMain main memory simulator to evaluate the proposed solution. (*check publication section)*

BSc. Internship **Cairo**

Si-Ware Systems, Egypt *Oct 2013 – June 2014*

Implementation & Verification of TMS320C25 DSP Core

My graduation project was an internship to implement an ASIC DSP core for a Texas Instrument open architecture. I was part of the verification team developing assembly based test cases, running RTL tests and GLS debugging, and STA analysis.

Education

University of British Columbia

PhD in Computer Engineering *2020–now*

University of British Columbia

MSc in Computer Engineering , Grade: 88% *2018–2020*

Alexandria University

BSc in Electronics and Communication Engineering , Grade: 78% *2010–2014*

Publications

1. Mohamed Matar. Design exploration of faster than nyquist equalizer system. Master's thesis, University of British Columbia, 2020

2. M. O. Matar, M. Jana, J. Mitra, L. Lampe, and M. Lis. A turbo maximum-a-posteriori equalizer for faster-than-nyquist applications. In *2020 IEEE 28th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, pages 167–171, 2020

3. M. A. Ewais, M. A. Omran, A. Raafat, and Y. Alkabani. A virtual memory architecture to enhance stt-ram performance as main memory. In *2016 IEEE Canadian Conference on Electrical and Computer Engineering (CCECE)*, pages 1–6, 2016

Teaching Experience

- (CPEN 311) Digital Systems Design, University of British Columbia.(T2'18,T1'19, T2'19,T1'20)
- (CSCE 231) Computer Organization, American University of Cairo.(Fall'15)

Technical skills

- **Programming Languages:** C/C++, Python, MATLAB, Bash.
- **System Simulators:** Intel Pin, SimpleScalar, Gem5.
- **Frameworks:** CUDA, Tensorflow, MxNet
- **Digital Design Skills:** VHDL , Verilog , System Verilog, UVM.
- **EDA:** Xilinx Vivado , Altera Quartus, Cadence IES, Synopsis VCS/Verdi, Modelsim .

References

References are available upon request.